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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/733,401	12/08/2000	James Murray	003242.P014	1880

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EXAMINER

SCHNEIDER, JOSHUA D

ART UNIT	PAPER NUMBER
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2182

DATE MAILED: 06/05/2003

8

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/733,401

Applicant(s)

MURRAY ET AL.

Examiner

Joshua D Schneider

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 19 May 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1, 2, 6, 12-16, 21 and 22 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1, 2, 6, 12-16, and 21-22 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 7.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

**DETAILED ACTION**

***Election/Restrictions***

1. Applicant's election of Group I, including claims 1, 2, 6, 12-16, and 21-23, in Paper No. 6 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

***Claim Rejections - 35 USC § 112***

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 21-23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. These claims depend from a cancelled claim of Group II and are need to be cancelled or amended so that they are dependent from claims of Group I and do not include subject matter of the restricted Group II with a normal and descriptor.

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1, 2, 6, and 12-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,809,335 to Kamiya in further view of the applicant admitted prior art (AAPA).

With regards to claim 1, Kamiya teaches a direct memory access (DMA) controller (Fig. 2,

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element 13, of Fig. 1, element 1, and column 3, lines 45-54), external modules (Fig. 1, elements 4, 6, and 8), and the termination of a DMA transfer (column 8, lines 30-41). Kamiya does not explicitly teach the external modules being I/O devices, but this is taught to be well known by the AAPA (page 2, lines 13-18). Kamiya teaches the DMA transfer being terminated by an interrupt, and is silent about a terminal count not having been reached. It would have been obvious to one of ordinary skill in the art at the time of invention that the terminal count could not have been reached or the transfer would not have to be restarted.

6. With regards to claim 2, Kamiya teaches the re-execution of a DMA transfer (column 8, lines 47-50) with an I/O device (external module).

7. With regards to claim 6, Kamiya teaches a system interconnect (Fig. 1, element 1), coupled to the I/O device (external modules, Fig. 1, elements 6 and 8) and a DMA controller (Fig. 2, element 13, of Fig. 1, element 1), a CPU coupled to the system interconnect (Fig. 1 elements 3 and 1), and a external modules coupled to the system interconnect (Fig. 1, elements 4, 6, and 8). It would have been obvious to one of ordinary skill in the art at the time of invention that the one of the external modules would have to be a memory device in order for the DMA transfer to be a memory access, as defined.

8. With regards to claim 12, Kamiya teaches a direct memory access (DMA) controller (Fig. 2, element 13, of Fig. 1, element 1, and column 3, lines 45-54), external modules (Fig. 1, elements 4, 6, and 8), and the termination of a DMA transfer (column 8, lines 30-41). Kamiya does not explicitly teach the external modules being I/O devices, though this is taught to be well known by the AAPA (page 2, lines 13-18). Kamiya teaches the re-execution of a DMA transfer (column 8, lines 47-50) with an I/O device (external module).

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9. With regards to claims 13 and 15, Kamiya teaches a direct memory access (DMA) controller to transfer data between and first and second device (Fig. 2, element 13, of Fig. 1, element 1, and column 3, lines 45-54), external modules (Fig. 1, elements 4, 6, and 8), and the termination of a DMA transfer (column 8, lines 30-41). Kamiya does not explicitly teach the external modules being I/O devices, though this is taught to be well known by the AAPA (page 2, lines 13-18). Kamiya teaches the termination of a DMA transfer (column 8, lines 30-41) with an I/O device (external module). Kamiya teaches the re-execution of a DMA transfer (column 8, lines 47-50) with an I/O device (external module). The use of acknowledge signals is not explicitly taught by Kamiya. However, the AAPA teaches that it is well known to use acknowledge signals to acknowledge control signal from an I/O device (page 2, lines 13-18). It would have been obvious to one of ordinary skill in the art at the time of invention, to use the well known request and acknowledge control signal lines of the AAPA with the termination and re-execution of Kamiya to create a system which can terminate and re-start DMA transfers, in order to provide a more robust I/O system which can handle CPU interrupts without causing fatal errors in a transfer currently being processed, and will provide greater system stability.

10. With regards to claim 14, Kamiya teaches the reloading the configuration registers with control information (column 8, lines 43-46). It is inherent that this reloading would take place before the transmission of an acknowledge signal which would occur during the following restarting process.

11. With regards to claim 16, Kamiya teaches the reloading the configuration registers with control information (column 8, lines 43-46). It is inherent that this reloading would include the clearing of a well known transfer size counter within the DMA controller that would occur

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before the following restarting process of the DMA block transfers and the acknowledge signal to the first device to start the transfer.

*Conclusion*

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. U.S. Patent 5,481,756 to Kanno teaches the halting of an auto-initializing DMA controller including size and destination registers. U.S. Patent 5,381,538 to Amini et al. teaches the restarting of a DMA transfer including control registers and a backup system. U.S. Patent 5,655,151 to Bowes et al. teaches DMA transfer including control registers and counters. U.S. Patent 5,713,040 to Gillespie et al. teaches DMA transfer including linked control information.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joshua D Schneider whose telephone number is (703) 305-7991. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey A Gaffin can be reached on (703) 308-3301. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

JDS  
May 29, 2003



JEFFREY GAFFIN  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2100